Wincom Tech. CO., LTD.

The LCD(M) Specialist

6F, Block 105, Jing Di Industrial Park,
Fu Qiang Rd. Fu Tian, Shenzhen City,China.
Tel: 0086-755-83308729
Fax: 0086-755-83308659
E-mail: craig.jiang@wincomlcd.com

PART NO. : COG12864B

FOR MESSRS. : _____

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ACCEPTED BY: _____ PROPOSED BY: _____

RECORD OF REVISION

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3. General specifications

3.1 General specifications

PLEASE REFER TO:

"CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS (MS-10-10000)".

3.2 Quality Assurance and Warranty

PLEASE REFER TO:

"QUALITY ASSURANCE MANUL (MS-10-10001)".

3.3 This individual specification is prior to general specifications

4. Features

* Display Model: STN Positive , Transmissive;
* Color : Display dot : Blue;
  Back ground : yellow;

* Display Format : 128 x 64 dots with Icons;
* IC : NT 7532H;
* Interface Input Data : Series;
* Driving Method : 1/65 Duty, 1/9 bias;
* Viewing Direction: 6 o'clock;
* Back light : Pure Green

5. Mechanical Specs.

Please refer to the drawing.

6. Electrical characteristics

6.1 Absolute Max Rating

Item	Symbol	Standard Value			Unit
		Min.	Typ.	Max.	
Supply Voltage For Logic	V_{DD}-Vss	-0.3	-	+3.6	V
Supply Voltage For LCD Drive	V_0	-0.3	-	+13.5	V
Input Voltage	V_{IN}	-0.3	-	V_{DD}+0.3	V
Operating Temp.	T_{OP}	-20	-	+70	°C
Storage Temp.	T_{ST}	-30	-	+80	°C

6.2 Electrical characteristics;

Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic Supply Voltage		V_{DD} – Vss	-	2.5	3.0	3.5	V
LCD Drive Voltage (Recommended Voltage)		V_0 – Vss	-	8.3	8.8	9.3	V
Input Voltage	"H" Level	V_{IH}	-	0.8V_{DD}	-	V_{DD}	V
	"L" Level	V_{IL}		VSS	-	0.2V_{DD}	V
Output Voltage	"H" Level	V_{OH}	I_{OH}=-0.5mA I_{OL}=0.5mA	0.8V_{DD}	-	V_{DD}	V
	"L" Level	V_{OL}		V_{DD}	-	0.2 V_{DD}	V
Current Consumption		I_{DD}	-	-	0.51	1.0	mA

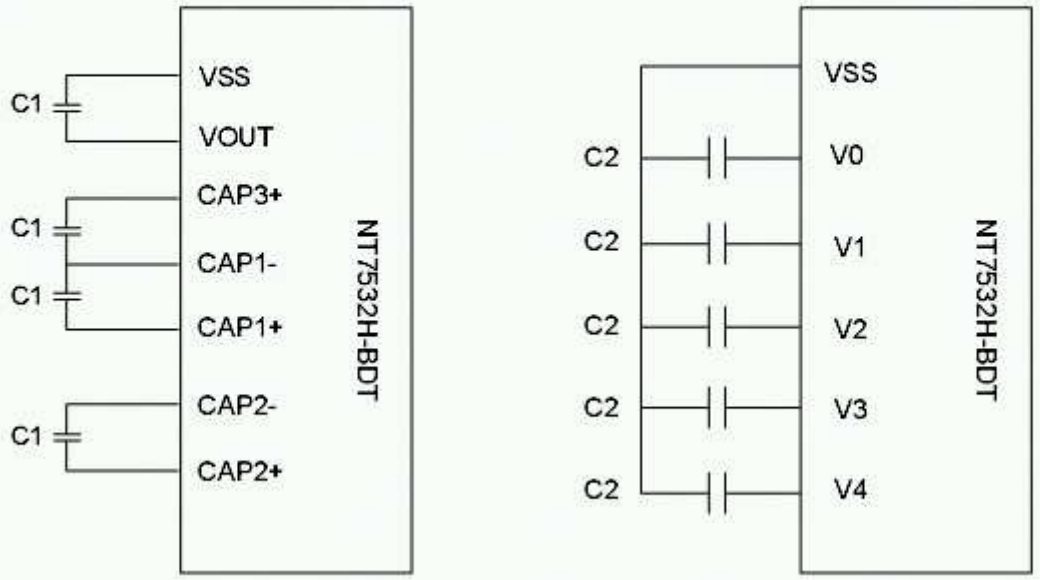
NOTE: 1) Duty Ratio=1/65, Bias Ratio=1/9

2) Measuring in Dots ON-state

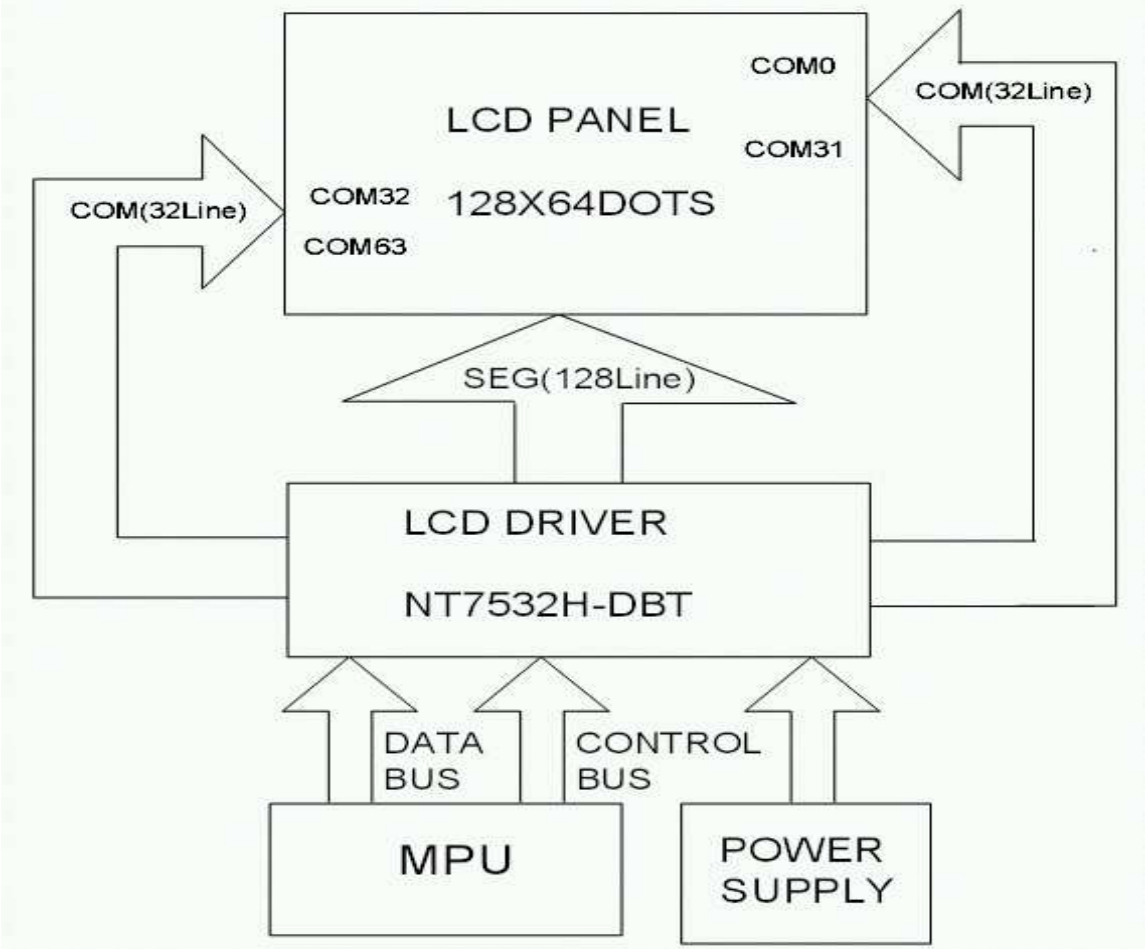
7. Power supply and block diagram

7.1 Power supply

Connect capacitor C1 between CAP1+ and CAP1-, between CAP2+ and CAP2-, between CAP1+ and CAP3-, and between VSS and VOUT , to produce a voltage level in the positive direction at the VOUT terminal that is 4 times the voltage level between VDD and VSS



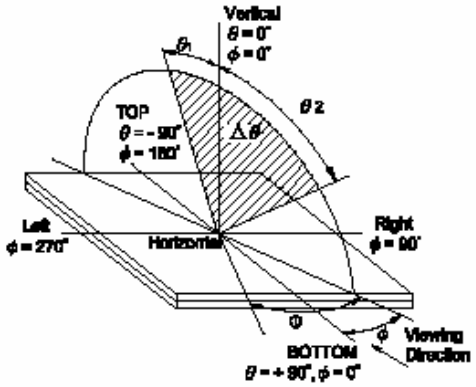
Note:C1=1.0~4.7 μ F,C2=0.47~1.0 μ F


LCD PANEL
COM0
COM31
COM32
COM63
128X64DOTS
COM(32Line)
COM(32Line)
SEG(128Line)
LCD DRIVER
NT7532H-DBT
DATA
BUS
CONTROL
BUS
MPU
POWER
SUPPLY

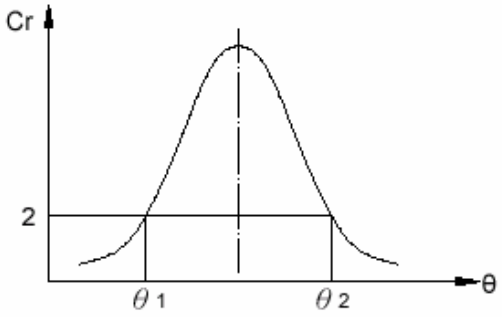
8. Electro – Optical Characteristics

Item	Symbol	Temp.	Min.	Typ.	Max.	Unit	Conditions	Note
Viewing Angle	Θ2 –Θ1	25℃	30	65	-	Deg.	-	1,2
	Φ		60	68	-			
Contrast Ratio	Cr	25℃	2	6.5	7.6	-	Θ=0° Φ=0°	3
Response Time(rise)	Tr	25℃	-	124	250	ms	Θ=0° Φ=0°	4
		0℃	-	950	1150			
Response Time(fall)	Tf	25℃	-	212	250	ms	Θ=0° Φ=0°	4
		0℃	-	950	1150			

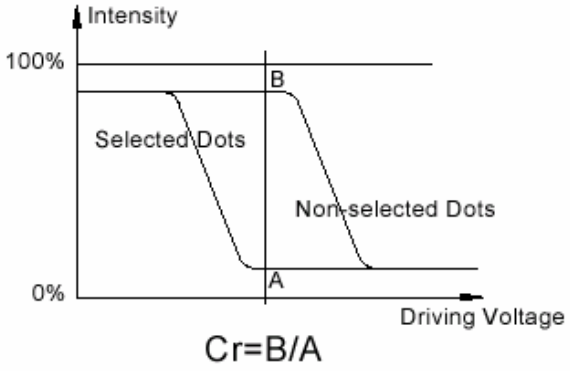
Note1 . Definition of Angle Θ&Φ



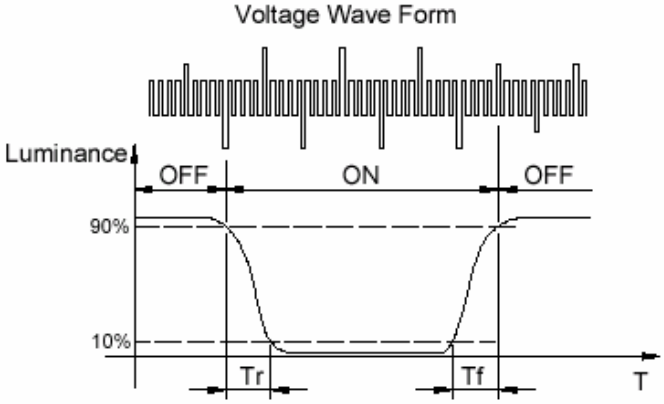
Note2. Definition of Viewing Angle Θ1&Θ2



Note3 . Definition of Contrast Cr



Note4. Definition of Optical Response



9.Interface Pin Assignment

PIN NO.	Symbol	Leve	Function
1	CS1B	L	Chip select
2	RES1B	L	Reset input pin
3	D/C	H/L	Register select input pin (Data/Instruction)
4	SCK	H/L	Serial input clock
5	SDA	H/L	Serial input data
6	VCC	3.0V	Power supply for lcm
7	GND	0V	Ground
8	LED-	0V	Power supply for LED
9	LED+	3V	Power supply for LED 15-20 mA
10	LED1 2-	0V	Power supply for LED1, LED2

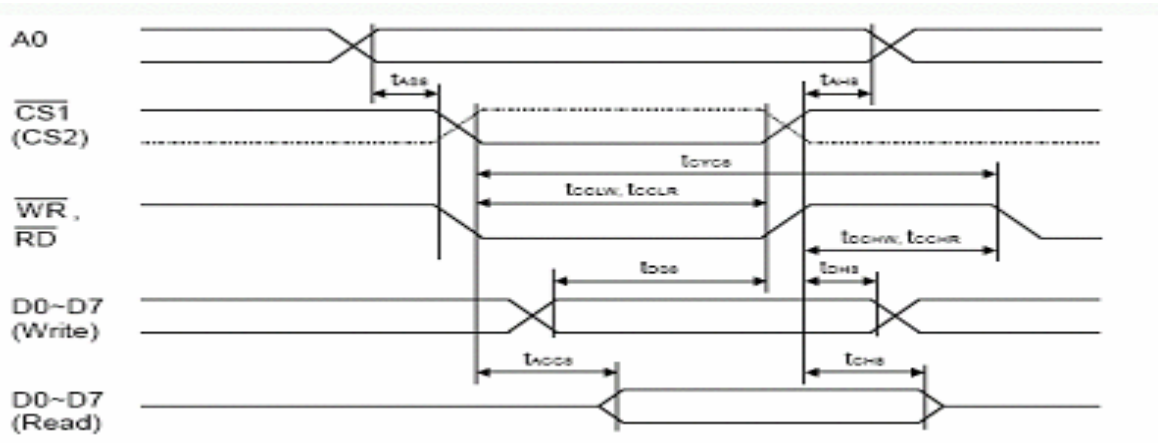
10.Command

Command	A0	RD	WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when goes high, and turn off when goes low
(2) Set Display Start Line	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Set Page Address	0	1	0	1	0	1	1	Page Address				B0h to BFh	Set the display data RAM page in Page Address register
(4) Set Column Address	0	1	0	0	0	0	1	Higher Column Address				00h to 1Fh	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Selects normal display (0) or entire display on
(11)Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Selects COM output scan direction *: invalid data
(16)Set Power Control	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Selects the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Selects internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	0	0	1	0	1	0	1	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
(22)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(23)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

11. Timing Character

8080 series

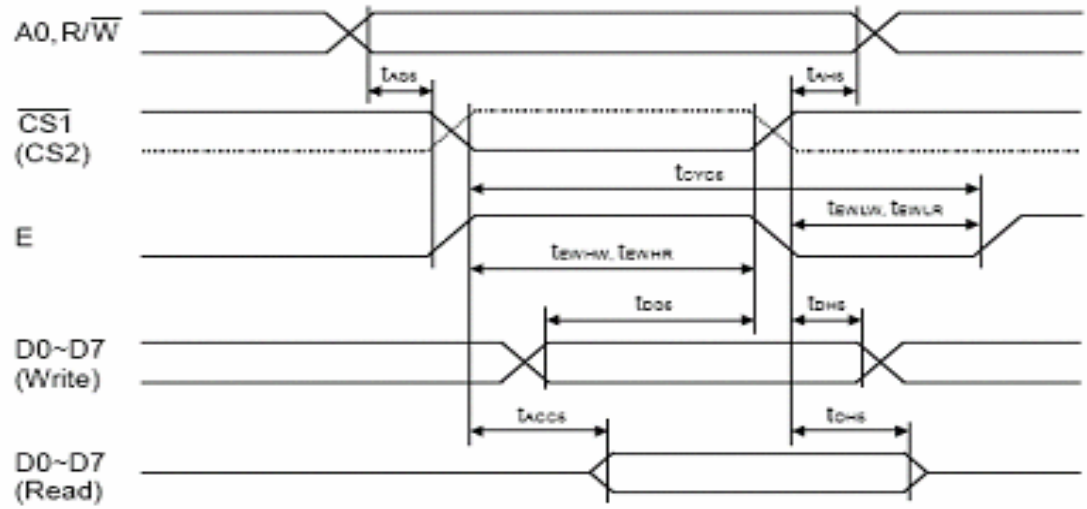


(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tAH8	Address hold time	0	-	-	ns	A0
tAS8	Address setup time	0	-	-	ns	
tCYC8	System cycle time	300	-	-	ns	
tCCLW	Control low pulse width (write)	90	-	-	ns	$\overline{WR}$
tCCLR	Control low pulse width (read)	120	-	-	ns	$\overline{RD}$
tCCHW	Control high pulse width (write)	120	-	-	ns	$\overline{WR}$
tCCHR	Control high pulse width (read)	60	-	-	ns	$\overline{RD}$
tDS8	Data setup time	40	-	-	ns	D0~D7
tDH8	Data hold time	15	-	-	ns	
tACC8	$\overline{RD}$ access time	-	-	140	ns	D0~D7, CL = 100pF
tCH8	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (tr, tf) is specified at 15ns or less.
(tr + tf) < (tCYC8 - tCCLW - tCCHW) for write, (tr + tf) < (tCYC8 - tCCLR - tCCHR) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. tCCLW and tCCLR are specified as the overlap interval when $\overline{CS1}$ is low (CS2 is high) and $\overline{WR}$ or $\overline{RD}$ is low.

68000 Series



(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tAHS	Address hold time	0	-	-	ns	A0
tAS	Address setup time	0	-	-	ns	
tCYCS	System cycle time	300	-	-	ns	
tEWHW	Control low pulse width (write)	90	-	-	ns	$\overline{WR}$
tEWHR	Control low pulse width (read)	120	-	-	ns	$\overline{RD}$
tEWLW	Control high pulse width (write)	120	-	-	ns	$\overline{WR}$
tEWLR	Control high pulse width (read)	60	-	-	ns	$\overline{RD}$
tDS	Data setup time	40	-	-	ns	D0~D7
tDHS	Data hold time	15	-	-	ns	
tACCS	$\overline{RD}$ access time	-	-	140	ns	D0~D7, CL = 100pF
tOHS	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (tr, tr) is specified at 15ns or less.
(tr + tr) < (tCYCS - tEWLW - tEWHW) for write, (tr + tr) < (tCYCS - tEWLR - tEWHR) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. tEWLW and tEWLR are specified as the overlap interval when $\overline{CS1}$ is low (CS2 is high) and E is high.

12.Mechanical Drawing